

## Preliminary program (March 9, 2026)

# 29th International Symposium on Design and Diagnostics of Electronic Circuits and Systems

Date: Monday, 27/Apr/2026

8:00am	Registration
-	
9:00am	
9:00am	Opening Session
-	
9:30am	
9:30am	<b>Keynote 1: Quantum Computing Is Coming: Why We Now Need Design and Diagnostics Expertise</b>
-	Rober Wille (Technical University of Munich, Munich Quantum Software Company, and Software Competence Center Hagenberg GmbH)
10:30am	
10:30am	CB1
-	
11:00am	
11:00am	S1: Digital design and security
-	
12:30pm	<b>A SAT-hard Compound Logic Locking Scheme with Empirical Resistance to Known Structural Attacks</b> Sonali Shukla <sup>1</sup> , Govind Jadhav <sup>1</sup> , Durgesh Sardan <sup>1</sup> , Suryakant Toraskar <sup>1</sup> , Jaynarayn Tudu <sup>2</sup> , Makoto Ikeda <sup>3</sup> , Masahiro Fujita <sup>3</sup> , Virendra Singh <sup>1</sup> 1: Indian Institute of Technology Bombay, India; 2: Indian Institute of Technology Tirupati, India; 3: The University of Tokyo, Japan
	<hr/>
	<b>Evaluating Communication and Architectural Overheads in NTT Accelerators for ML-KEM</b> Stefano Di Matteo <sup>1,2</sup> , Emanuele Valea <sup>2</sup> 1: Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France; 2: Univ. Grenoble Alpes, CEA, List, F-38000 Grenoble, France
	<hr/>
	<b>Periphery-Aware Power Side-Channel Hardening for Digital CIM-BNN Accelerators</b> Fouwad Jamil Mir <sup>1,2</sup> , Abdullah Aljuffri <sup>1</sup> , Said Hamdioui <sup>1,2</sup> , Mottaqiallah Taouil <sup>1,2</sup> 1: Delft University of Technology, The Netherlands; 2: CognitivelC, Delft, The Netherlands
	<hr/>
	<b>MTBT: Multi-Target Bit Trojan Attack for Quantized Neural Networks</b> Akiha Kusumoto, Mohammad Hasan Ahmadilivani, Jaan Raik Tallinn University of Technology, Estonia
12:30pm	LB1
-	
2:00pm	
2:00pm	S2: Dependability and test
-	
3:30pm	<b>Experimental Analysis of FreeRTOS Dependability through Targeted Fault Injection Campaigns</b> Luca Mannella, Stefano Di Carlo, Alessandro Savino Politecnico di Torino, Italy
	<hr/>
	<b>Reliability Assessment in Approximate Accelerator Synthesis</b> Somayeh Sadeghi-Kohan <sup>1</sup> , Muhammad Awais <sup>1</sup> , Qazi Arbab Ahmed <sup>2</sup> , Marco Platzner <sup>1</sup> , Sybille Hellebrand <sup>1</sup> , Thorsten Jungeblut <sup>2</sup> , Hans-Joachim Wunderlich <sup>3</sup>

1: Paderborn University, Paderborn, Germany; 2: ReMi Research Group, University of Applied Sciences and Arts Bielefeld, Bielefeld, Germany; 3: University of Stuttgart, Stuttgart, Germany

---

### **On-Chip Sensor with Programmable Delay Logic to Monitor Memory Aging Evolution**

**Fabian Luis Vargas<sup>1</sup>, Vache Galstyan<sup>2</sup>, Gurgen Harutyunyan<sup>3</sup>, Yervant Zorian<sup>4</sup>**

1: IHP – Leibniz Institute for High Performance Microelectronics, Germany; 2: Synopsys, USA; 3: Synopsys, USA; 4: Synopsys, USA

---

### **Ambient Parametric Test Reduction in Post-Silicon Production Testing via Temperature-Dependent Modelling: Three Approaches and a Case Study**

**Bianca Carbusescu-Stoenescu<sup>1</sup>, Emilian David<sup>2</sup>, Mihai Popovici<sup>3</sup>, Marina Topa<sup>1</sup>, Valentina Davidoiu<sup>3</sup>, Andi Buzo<sup>4</sup>, Georg Pelz<sup>4</sup>**

1: Technical University of Cluj Napoca, Romania; 2: Institute of Computer Science, Romanian Academy, Iasi Branch, Romania; 3: Infineon Technologies, Bucharest, Romania; 4: Infineon Technologies, AG Neubiberg, Germany

---

3:30pm

**Posters + CB2: Poster session**

5:00pm

### **A Framework for Chiplet Authentication During Post-Stacking Test**

**Juan Suzano<sup>1</sup>, Anthony Philippe<sup>3</sup>, Fady Abouzeid<sup>2</sup>, Giorgio Di Natale<sup>1</sup>, Philippe Roche<sup>2</sup>**

1: TIMA; 2: ST Microelectronics; 3: CEA

---

### **A Model-Driven Approach to Variable-Frequency Clock Synthesis for PSN-Resilient IC Wake-Up**

**Vipin Kumar Singh<sup>1</sup>, Vijay Pratap Yadav<sup>1</sup>, Vassilis Alimisis<sup>2,3</sup>, Paul P Sotiriadis<sup>2,3</sup>, Shubhankar Majumdar<sup>4</sup>, Alak Majumder<sup>1</sup>**

1: NIT Arunachal Pradesh, India; 2: Archimedes, Athena Research Center, Marousi, Greece; 3: National Technical University of Athens, Greece; 4: NIT Meghalaya, India

---

### **Ageing Monitoring for Commercial Microcontrollers Based on Timing Windows**

**Leandro Lanzieri<sup>1,2,3</sup>, Jiri Kral<sup>1</sup>, Goerschwin Fey<sup>2</sup>, Holger Schlarb<sup>1</sup>, Thomas C. Schmidt<sup>3</sup>**

1: Deutsches Elektronen-Synchrotron DESY, Germany; 2: Hamburg University of Technology, Germany; 3: Hamburg University of Applied Sciences, Germany

---

### **ANN-Based Ultra Fast Synthesis of Flash ADCs**

**Hakan Taşkıran, Abdullah Bayram, Engin Afacan**

Gebze Technical University, Turkey (Türkiye)

---

### **Approximated MAGIC-ReRAM Adder Circuits for Low-Latency In-Memory Computing**

**Saeideh Nabipour<sup>1</sup>, Chandan Kumar Jha<sup>2</sup>, Saeideh Shirinzadeh<sup>1,3</sup>, Rolf Drechsler<sup>1,2</sup>**

1: Cyber-Physical Systems, DFKI GmbH, Germany; 2: University of Bremen, Germany; 3: Fraunhofer Institute for Systems and Innovation Research (ISI), Karlsruhe, Germany

---

### **Comparative Analysis of Hardware Accelerator Architectures for Performance and Energy Efficient Deep Neural Network Execution**

**Salsabil Saoudi<sup>1</sup>, Mario Barbareschi<sup>2</sup>, Alberto Bosio<sup>1</sup>**

1: Ecole Centrale de Lyon, INSA Lyon, CNRS, Université Claude Bernard Lyon 1, CPE Lyon, INL (UMR 5270), 69130 Ecully, France; 2: University of Naples Federico II, Department of Electrical Engineering and Information Technologies, 80125 Naples, Italy

---

### **Efficient Co-Design of Networked Control Systems with 5G Configured Grant Scheduling**

**Yungang Pan<sup>1</sup>, Max Nyberg Carlsson<sup>2</sup>, Soheil Samii<sup>1</sup>, Petru Eles<sup>1</sup>, Zebo Peng<sup>1</sup>**

1: Embedded Systems Lab, Linköping University, Sweden; 2: Department of Automatic Control, Lund University, Sweden

---

### **Error Injecting Circuit: an Alternative to Discrete Gaussian Samplers**

**Andrea Marengo<sup>1</sup>, Emanuele Valea<sup>1</sup>, Elena Ioana Vatajelu<sup>2</sup>**

1: CEA List; 2: TIMA-CNRS

---

### **Fan-In Aware Graph-Based Optimization for MAC-Based In-Memory Computing**

**Fatemeh Shirinzadeh<sup>1</sup>, Abhoy Kole<sup>1</sup>, Kamalika Datta<sup>1,2</sup>, Saeideh Shirinzadeh<sup>1,3</sup>, Rolf Drechsler<sup>1,2</sup>**

1: German Research Centre for Artificial Intelligence (DFKI), Germany; 2: Institute of Computer Science, University of Bremen, Germany; 3: Fraunhofer Institute for Systems and Innovation Research (ISI), Germany

---

### **Monolithic quantum random number generator containing Si-LED, SPAD and analog processing**

**Horst Zimmermann, David Bugl, Bernhard Goll, Michael Hofbauer, Kerstin Schneider-Hornstein, Hiwa Mahmoudi**

TU Wien, Austria

---

### **Pulsed Electromagnetic Fault Injection on RO-based True Random Number Generators in FPGAs**

**Sami El Amraoui<sup>1</sup>, Mahdi Allaw<sup>1</sup>, Florian Pebay-Peyroula<sup>2</sup>, Régis Leveugle<sup>1</sup>, Paolo Maistri<sup>1</sup>**

1: Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA; 2: CEA-Leti

---

### **Security-Aware Benchmarks for Performance Exploration of CHERI-Enabled Architectures**

**Spandan Das<sup>1</sup>, Sayak Deb<sup>2</sup>, Khushboo Qayyum<sup>3</sup>, Sallar Ahmadi-Pour<sup>1</sup>, Christoph Lüth<sup>1,3</sup>, Rolf Drechsler<sup>1,3</sup>**

1: Institute of Computer Science, University of Bremen, Bremen, Germany; 2: Institute of Physics and Electrical Engineering, University of Bremen, Bremen, Germany; 3: Cyber-Physical Systems, DFKI GmbH, Bremen, Germany

---

### **BLAR-3D: Beta-Regulated Learning-Based Adaptive Routing for 3D Network-on-Chip**

**Cevdet Aslan, Suleyman Tosun**

Hacettepe University, Turkey (Türkiye)

---

### **Influence of Temperature Variations on the Frequency of Two-dimensional MEMS Mirrors**

**Marlene Alexandra Schneider<sup>1,2</sup>, Norbert Druml<sup>2</sup>, David Brunner<sup>2</sup>**

1: Technische Universität Graz; 2: Infineon Technologies Austria AG

---

5:00pm

**S3: Analog circuits**

6:30pm

### **A Wideband Q/V Band Cascode Darlington Power Amplifier using Transmission Line Transformer and Current-reuse Techniques**

**Chin-Wei Kuo<sup>1</sup>, Hsin-Chieh Lin<sup>2</sup>, Chien-Nan Kuo<sup>3</sup>, Hwann-Kaeo Chiou<sup>1</sup>**

1: National Central University, Taoyuan, Taiwan; 2: Taiwan Semiconductor Research Institute, National Institutes of Applied Research, Hsinchu, Taiwan; 3: National Yang Ming Chiao Tung University, Hsinchu, Taiwan

---

### **A 320.3 fJ/bit UCle Advanced Package TX Driver in 28 nm FDSOI**

**Patryk Kozicki<sup>1</sup>, Viki Szortyka<sup>1</sup>, Witold Pleskacz<sup>2</sup>**

1: Cadence Design Systems, Poland; 2: Warsaw University of Technology, Institute of Microelectronics & Optoelectronics

---

### **Integrated Gate Driver with Adaptive Dead-Time Control and Gate-Drive Boost for High-Efficiency BCD Synchronous Buck Converters**

**Fahd Khan<sup>1</sup>, Niccolo' Brambilla<sup>2</sup>, Sandro Rossi<sup>2</sup>, Calogero Ribellino<sup>3</sup>, Edoardo Bonizzoni<sup>1</sup>, Piero Malcovati<sup>1</sup>**

1: Department of Electrical, Computer and Biomedical Engineering, University of Pavia, Italy; 2: STMicroelectronics, Smart Power TR&D, Castelletto, Italy; 3: STMicroelectronics, R&D, Catania, Italy

---

### **Silicon-Proven Low-Dropout Regulator Designed in 65nm CMOS Technology**

**David Maljar, Róbert Ondica, Daniel Arbet, Martin Kováč, Viera Stopjková**

Slovak University of Technology, Faculty of Electrical Engineering and Information Technology, Slovak Republic

**6:30pm**

**ET1: Embedded tutorial**

-

**7:30pm**

**AI vs. Verification Engineer: Fight or Synergy?**

**Marcela Zachariášová**

Brno University of Technology, Czech Republic (Czechia)

**8:00pm**

**WR: Welcome reception**

-

**10:00pm**

Date: Tuesday, 28/Apr/2026

9:00am	<b>Keynote 2: Heterogeneous Integration in AI Computing: Challenges and Solutions</b>
-	Leticia Maria Bolzani Pöhls (IHP GmbH, Leibniz Institute for High Performance Microelectronics, Frankfurt (Oder), Germany)
10:00am	
10:00am	<b>S4: Security and optimization</b>
-	
11:00am	<b>Assessing the Vulnerability of Open-Source RISC-V Processors to Transient Execution Attacks</b>
	Elia Lazzeri <sup>1</sup> , Gianluca Furano <sup>2</sup> , Luca Cassano <sup>1</sup>
	1: Politecnico di Milano, Italy; 2: European Space Agency, The Netherlands
	<hr/>
	<b>Measurement-Driven Adaptive Low-Overhead Implementation of Multi-Controlled Toffoli Gates</b>
	Abhoy Kole <sup>1</sup> , Till Schnittka <sup>2</sup> , Rolf Drechsler <sup>1,2</sup>
	1: DFKI, Germany; 2: University of Bremen, Germany
	<hr/>
	<b>Co-Optimizing Performance and Security of Analog Integrated Circuits</b>
	Abdullah Bayram <sup>1</sup> , Haralampos-G. Stratigopoulos <sup>2</sup> , Engin Afacan <sup>1</sup>
	1: Gebze Technical University, Turkey (Türkiye); 2: Sorbonne Université, CNRS, LIP6 (France)
11:00am	<b>CB3</b>
-	
11:30am	
11:30am	<b>S5: Analog circuits - ANN, IoT and CAD SW</b>
-	
12:30pm	<b>A Power-Efficient Analog Hardware Swish-Based Artificial Neural Network Architecture for Star Evolutionary Phase Classification</b>
	Andreas Papathanasiou <sup>1</sup> , Vassilis Alimisis <sup>2</sup> , Alak Majumder <sup>3</sup> , Paul P. Sotiriadis <sup>1</sup>
	1: National Technical University of Athens; 2: Archimedes, Athena Research Center, Greece; 3: National Institute of Technology, Arunachal Pradesh, Pin-791113, India
	<hr/>
	<b>A CMOS 72kHz–123MHz Tunable Oscillator for Low-Power IoT Applications</b>
	Robert Ondica, Daniel Arbet, Martin Kováč, Miroslav Potočný, Viera Stopjaková
	Slovak University of Technology in Bratislava, Slovak Republic
	<hr/>
	<b>CAD Software for the Detection of Floating Metals for Advanced CMOS Technologies</b>
	Sweekriti Patle <sup>1</sup> , Marika Grochowska <sup>1</sup> , Witold Pleskacz <sup>2</sup>
	1: Cadence Design System, Poland; 2: Warsaw University of Technology, Poland
12:30pm	<b>LB2</b>
-	
2:00pm	
2:00pm	<b>Special Session</b>
-	
3:30pm	<b>Optimizing Edge AI: Current Challenges and the Neuromorphic Outlook</b>
	Milan Dinčić <sup>1</sup> , Davide Bertozzi <sup>2</sup> , Alice Bizzarri <sup>3</sup> , Rizwan Tariq Syed <sup>4</sup> , Edward Jones <sup>2</sup>
	1: University of Niš, Faculty of Electronic Engineering, Serbia; 2: University of Manchester, United Kingdom; 3: University of Ferrara, Italy; 4: IHP – Leibniz-Institut für innovative Mikroelektronik, Frankfurt (Oder), Germany
3:30pm	<b>CB4</b>
-	
4:00pm	
4:30pm	<b>SEGD: Social event, gala dinner</b>
-	
10:00pm	

Date: Wednesday, 29/Apr/2026

9:00am **Keynote 3: Scaling EDA for Increasing System Complexity: Lessons Learned and Future Directions**

- Karel Masařík (Director of Czech Semiconductor Centre)

10:00am

10:00am **S6: Hardware accelerators**

-

11:00am

**DP-MCTS: Deep Payout-Driven MCTS for Approximate Accelerator Design**

Muhammad Awais<sup>1</sup>, Hassan Ghasemzadeh Mohammadi<sup>2</sup>, Sayed Morteza Jawadi<sup>1</sup>, Marco Platzner<sup>1</sup>

1: Paderborn University, Paderborn Germany; 2: Reneo Group GmbH, Hamburg, Germany

---

**FRAPPE: Feasibility Report on Accelerating Payload Pattern-matching Engines in Intrusion Detection Systems with FPGAs**

Lukas Sismis<sup>1</sup>, Jan Korenek<sup>2</sup>

1: CESNET z. s. p. o., Czech Republic (Czechia); 2: Faculty of Information Technology, Brno University of Technology

---

**A Parallel FPGA Architecture for Data Clustering using the Potts Model**

Xingjian Gao, Jie Han

University of Alberta, Canada

11:00am

CB5

-

11:30am

11:30am **S7: Analog circuits**

-

12:30pm

**Investigation of MPPT Control for Hybrid Voltage Converter in Low-Power Energy Harvesters**

Martin Kováč, Róbert Ondica, Richard Bagín, Daniel Arbet, Viera Stopjaková

Slovak University of Technology in Bratislava, Slovak Republic

---

**Conditional Variational Autoencoders for Statistical MOSFET Modeling**

Dawid Sudowski<sup>1</sup>, Dominik Kasprowicz<sup>2</sup>

1: Rail-Mil Sp. z o.o., 03-994 Warsaw, Poland; 2: Warsaw University of Technology, 00-665 Warsaw, Poland

---

**Harmonic-Controlled Bandpass Filter With Upper Stopband Suppression for 6G Applications**

Sanghoon Jeong, Juseop Lee

College of Informatics, Korea University, Seoul, South Korea

12:30pm

ET2: Embedded tutorial

-

1:30pm

**Considerations on the Design of Resilient 2.5-3D Heterogeneous, Multilayer Interposer Systems for Chip Lifecycle Management**

Fabian Luis Vargas

IHP – Leibniz Institute for High Performance Microelectronics, Germany

1:30pm

BPA and Closing

-

2:00pm

2:00pm

LB3

-

3:00pm